

APQO 7050

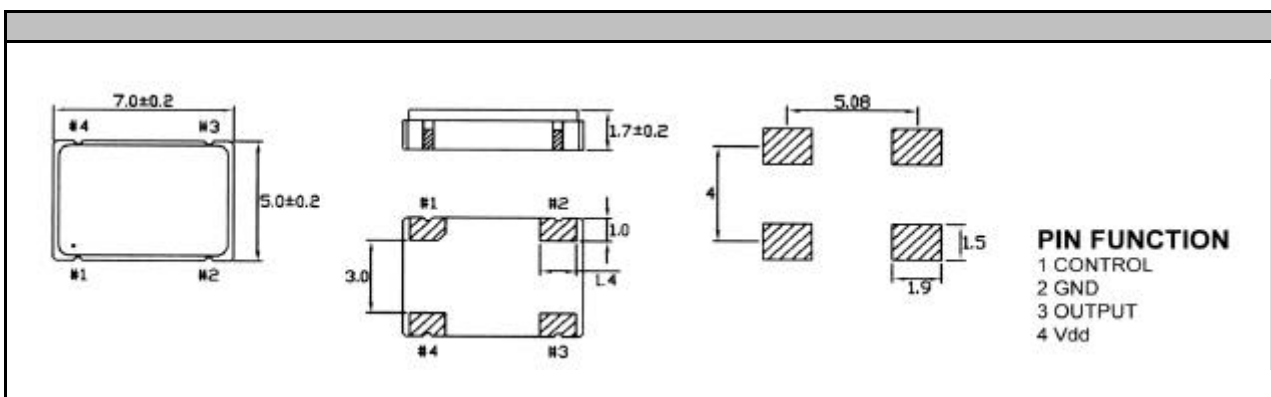
Features/Merkmale

- Standard DIL 8
- Low Cost to Performane
- 3.0 - 5.5 Volt Available
- Tolerance and Stability to ± 25 ppm



Specifications:				
Description	Min	Typ	Max	Unit
Frequency Range:	1.000		133.000	MHz
Available Stability Options:	-25		25	ppm
	-50		50	ppm
	-100		100	ppm
Programmable Supply Voltage:				
(1-133 MHz)	4.5	5.0	5.5	V
(1-133 MHz)	3.0	3.3	3.6	V
Operating Temperature Range Options:				
	0		+70	°C
	-40		+85	°C
Storage Temperature:				
	-55		+125	°C
Aging (PPM / Year), Ta = 25C, Vdd = 5 / 3.3 V			± 5	
Programmable Output Level:	TTL / CMOS			

Operating Conditions:			
Description	Min	Max	Unit
Vdd Supply Voltage	3.0	5.5	V
CTTL Max Capacitive Load on outputs for TTL levels			25
	4.5 V - 5.5 V Vdd \leq 40 MHz	50	pF
	4.5 V - 5.5 V Vdd > 40 - 133 MHz	25	pF
CCMOS Max Capacitive Load on outputs for CMOS levels			
	4.5 V - 5.5 V Vdd \leq 66 MHz	50	pF
	4.5 V - 5.5 V Vdd > 66 - 133 MHz	25	pF
	3.0 V - 3.6 V Vdd \leq 40 MHz	30	pF
	3.0 V - 3.6 V Vdd > 40 - 100 MHz	15	pF



Dimensions/Abmessungen in mm

Electrical Characteristics					
Description	Test Conditions	Min	Typ	Max	Unit
Input Characteristics (Pin 1): V _{IL} , Low-Level Input Voltage TO TRI_STATE OR POWER DOWN	4.5 - 5.5 V V _{dd} 3.0 - 3.6 V V _{dd}			0.8 0.2 V _{dd}	V V
V _{IH} , High-Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT	4.5 - 5.5 V V _{dd} 3.0 - 3.6 V V _{dd}	2.0 0.7 V _{dd}			V V
I _{IL} , Input Low Current I _{IH} , Input High Current	V _{IN} = 0V V _{IN} = V _{dd}			10 5	μA μA
Input Characteristics: V _{OL} , Low-Level Output Voltage	4.5 V - 5.5 V V _{dd} , 16 mA I _{oL} 3.0 V - 3.6 V V _{dd} , 8 mA I _{oL}			0.4 0.4	V V
V _{OHTTL} , High-Level Output Voltage TTL	4.5 V - 5.5 V V _{dd} , -16 mA I _{oL}	2.4			V
V _{OHCOS} , High-Level CMOS Voltage	4.5 - 5.5 V _{dd} , -16 mA I _{oL} 3.0 V - 3.6 V V _{dd} , -8 mA I _{oL}	V _{dd} - 0.4 V _{dd} - 0.4			V V
Power Supply Current: (unloaded)	4.5 - 5.5 V _{dd} , OUTPUT FREQ ≤ 133 MHz 3.0 - 3.6 V _{dd} , OUTPUT FREQ ≤ 100 MHz			45 25	mA mA
Standby Current:			10	50	μA
Input Pull-Up Resistor (PIN 1)	4.5 - 5.5 V _{dd} , V _{IN} = 0V 4.5 - 5.5 V _{dd} , V _{IN} = 0.7 V	1.1 50	3.0 100	8.0 200	MΩ KΩ
Tri-State Leakage Current:	5.0 V _{dd}		20		μA
Output Enable Mode:	Output is Tri-States				
Power Down Mode:	Output is Tri-States				

Output Clock Switching Characteristics					
Description	Test Conditions	Min	Typ	Max	Unit
Duty Cycle: TTL @ 1.4 V 4.5 - 5.5 V _{dd}	≤ 50 MHz, C _L = 50 pF 50 - 66 MHz, C _L = 15 pF 66 - 125 MHz, C _L = 25 pF 125 - 133 MHz, C _L = 15 pF	45 45 40 40		55 55 60 60	% % % %
Duty Cycle: CMOS @ V _{dd} / 2 4.5 - 5.5 V _{dd} 3.0 - 3.6 V _{dd}	≤ 66 MHz, C _L ≤ 25 pF 66 - 125 MHz, C _L ≤ 25 pF 125 - 133 MHz, C _L ≤ 15 pF ≤ 40 MHz, C _L ≤ 30 pF 40 - 100 MHz, C _L ≤ 15 pF	45 40 40 45 40		55 60 60 55 60	% % % % %
Output Clock Rise / Fall:	0.8 V - 2.0 V, 4.5 - 5.5 V _{dd} , C _L = 50 0.8 V - 2.0 V, 4.5 - 5.5 V _{dd} , C _L = 25 0.8 V - 2.0 V, 4.5 - 5.5 V _{dd} , C _L = 15 0.2 - 0.8 V _{dd} , 4.5 - 5.5 V _{dd} , C _L = 50 0.2 - 0.8 V _{dd} , 3.0 - 3.6 V _{dd} , C _L = 30 0.2 - 0.8 V _{dd} , 3.0 - 3.6 V _{dd} , C _L = 15			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
Start Up Time	From power on			10	ms
Power Down Delay Time Synchronous / Asynchronous	PWR_DWN pin LOW to output Hi-Z		T / 2 10	T+10 15	ns ns
Output Disable Time Synchronous / Asynchronous	OE pin LOW to output Hi-Z T = Frequency oscillator period		T / 2 10	T+10 15	ns ns
Output Enable Time				100	ns
Period Jitter: S	≤ 33.000 MHz > 33.000 MHz		11 11	13 17	ps ps
Peak to Peak	≤ 33.000 MHz > 33.000 MHz		83 83	100 110	ps ps

Remarks/Bemerkungen:

All specifications subject to change without notice. / Wir behalten uns vor, Daten ohne Mitteilung zu ändern.